Subject Description Form

Subject Code	EIE511
Subject Title	VLSI System Design
Credit Value	3
Level	5
Pre-requisite/ Co-requisite/ Exclusion	Logic Design
Objectives	To provide an understanding of various aspects of VLSI system design. In particular, to look at how different design methodologies and styles are utilized to achieve high-performance, cost-effective integrated circuits.
Intended Learning Outcomes	Upon completion of the subject, students will be able to: a. master the fundamental principles behind the design methodologies of digital systems in VLSI; b. know what the current state-of-the-art digital design technologies can offer; c. apply top-down, systematic design approach for high performance digital CMOS VLSI integrated circuit with HDL and electronic design automation software; d. design the digital VLSI systems to meet performance and time-to-market goals; e. derive feasible and efficient testing and design-for-testability structures to achieve high quality and short design turnaround. f. adopt GenAI tools in digital design to improve design quality and speed up design cycle.
Subject Synopsis/ Indicative Syllabus	**Part I: Fundamental Concepts** 1. Overview 1.1 Overview of different design methodologies. 1.2 Design styles (Gate Arrays, Standard Cells, Custom); future technology trends. 2. Semiconductor Technologies 2.1 Technology comparison - CMOS, BIPOLAR, NMOS, and Bipolar-CMOS. 2.2 Static and dynamic CMOS circuit design. 2.3 Basic elements of logic design. **Part 2: Design Methodology, Performance Evaluation and Testing** 3. Digital System Design 3.1 HDL design for arithmetic components: adders and related functions, binary counters, and multipliers. 3.2 HDL design for simple systems of computer arithmetic. 3.3 HDL design for real digital systems. 4. Major Design Issues 4.1 Logic levels, delay calculations, layout and parasitics. 4.2 Clocking methodologies, clock distribution and driving large load. 4.3 Layout consideration - importance of good floor-planning and its effect on overall chip performance. 4.4 Wiring strategies, device scaling, and power estimates; and low power design techniques. 4.5 Testability: Fault models and fault simulation. 5. Electronic Design Automation 5.1 Logic Synthesis and floor-planning.

5.2 Placement and routing.

Teaching/Learning Methodology

The theories and applications of various digital system design techniques will be discussed and explain in lectures. Laboratory sessions will be provided to strengthen students' understanding on the theories and hands-on design experiences on the applications. Students will also be requested to practise the implementation of a digital system in the project. Class discussion can help the students to have better understand of VLSI application among the discussions. Project can allow the students to design, implement and test a VLSI system.

Teaching/Learning Methodology	Intended Subject Learning Outcomes					
	a	b	c	d	e	f
Lectures	✓	✓	✓	✓		
Project			✓	✓	✓	✓
Class discussion		✓	✓	✓		
Laboratory sessions			✓	✓	✓	✓

Assessment Methods in Alignment with Intended Learning Outcomes

Specific assessment methods/tasks	% weighting	Intended subject learning outcomes to be assessed (Please tick as appropriate)					
		a	b	c	d	e	f
1. Laboratory exercises	10%	✓		✓	✓		✓
2. Assignments	20%	✓	✓				
3. Project	30%	✓		✓	✓		✓
4. Tests	40%	✓	✓		✓	✓	
Total	100%						

Explanation of the appropriateness of the assessment methods in assessing the intended learning outcomes:

1. **Laboratory Exercises**: For each lab session, students will need to understand the fundamental concepts [Outcome (a)] before they can complete the lab exercises. Because the lab sessions involve the digital design technologies [Outcome (c)] and the use of GenAI tools [Outcome (f)], students' ability to apply these technologies should be reflected based on the performance [Outcome (d)] of their design.
2. **Assignments:** Students will need to do the assignments in order to understand the fundamental concepts [Outcome (a)] and the current design methodologies [Outcome (b)] of digital VLSI system.
3. **Projects:** In the project, students will need to understand the fundamental concepts [Outcome (a)] before they can complete the project. Because the project involves the digital design technologies [Outcome (c)] and the use of GenAI tools [Outcome (f)], students' ability to apply these technologies should be reflected based on the performance [Outcome (d)] of their design.
4. **Tests:** Students will need to answer questions about the fundamental concepts [Outcome (a)] of various design technologies and their applications [Outcome (b)]. Limitations, performance [Outcome (d)] and testing procedure [Outcome (e)] of current digital system design technologies will also be asked in the test.

Student Study Effort Expected

Class contact:	
▪ Lectures	26 Hrs.
▪ Laboratory exercises	13 Hrs.
Other student study effort:	
▪ Project	44 Hrs.
▪ Revision and completion of assignments	30 Hrs.

	Total student study effort	113 Hrs.
Reading List and References	1. W. Wolf, *Modern VLSI Design – System-on-Chip Design*, Prentice Hall International, 2002. 2. Taraate Vaibbhav, Digital Logic Design Using Verilog : Coding and RTL Synthesis, 2nd edition, Springer, 2022. 3. Lata Tripathi, Suman, et al., Digital VLSI Design and Simulation with Verilog, Wiley, 2022. 4. N. Weste, K. Eshraghian, *Principles of CMOS VLSI Design - A Systems Perspective*, 2nd edition, Addison-Wesley, 1993.	

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